

11. The interface of claim ~~11~~10 wherein said latch inverts said latching node of
said latch to produce said output.

IN THE ABSTRACT:

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A static logic signal to dynamic logic interface that produces a monotonic output.

An inverse of a dynamic logic evaluate clock is fed to the clock input of a transparent
latch with clock and enable inputs. A delayed version of the inverse of the evaluate clock
is generated by a delay element. The delayed inverse of the evaluate clock is fed to the
10 enable input of the latch. The input to the latch comes from static logic and the output of
the latch is fed to the dynamic logic. The net result is a latch that is open until the
evaluate clock is instructing the dynamic logic to ~~reset~~ evaluate, and remains closed until
a delay element delay time after the evaluate clock instructs the dynamic logic to reset.